JEDEC

Global Standards for the Microelectronics Industry

DDR4 Mini Workshop

Server Memory Forum 2011

Disclaimer

- Even though Majority of DDR4 spec has been defined/Fixed, there might be chance of update before publicationt

- Rev A is expected to be in publice 1H'12 and the contents of this material might be changed in Final version

DDR4 Outlook

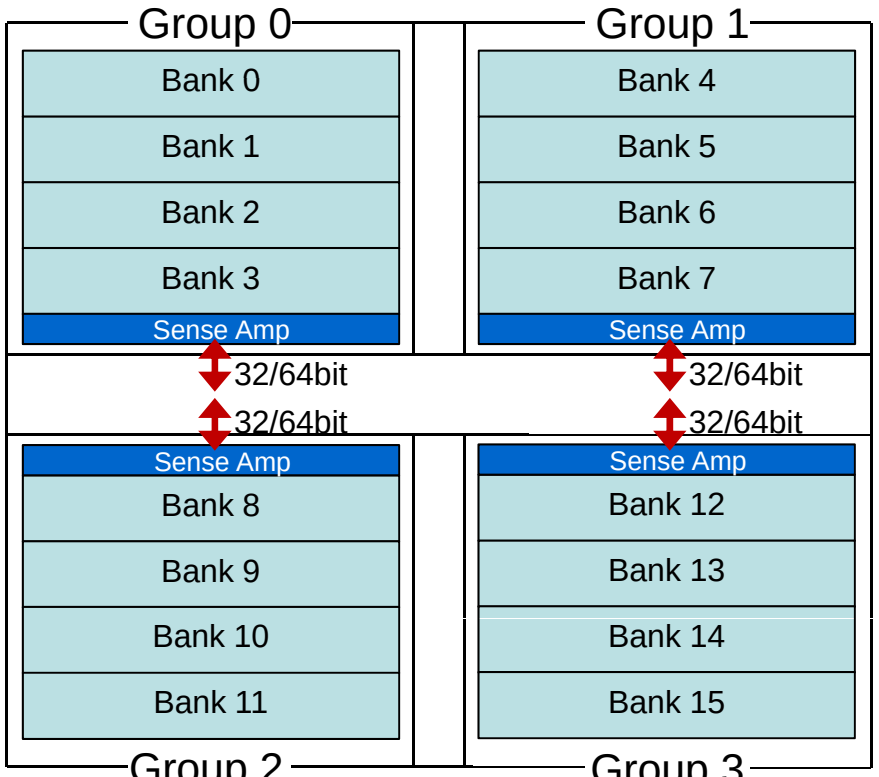
- DDR4 adopts evolutionary path with High BW & reliability scheme

Spec items		DDR3	DDR4
Density / Speed		512Mbp~8Gb 1.6~2.1Gbps	2Gb~16Gb 1.6~3.2Gbps
Interface	Voltage (VDD/VDDQ/VPP)	1.5V/1.5V/NA (1.35V/1.35V/NA)	1.2V/1.2V/2.5V
	Vref	External Vref (VDD/2)	Internal Vref (need training)
	Data IO	CTT (34ohm)	POD (34ohm)
	CMD/ADDR IO	CTT	CTT
	Strobe	Bi-dir / diff	Bi-dir / diff
Core architect	# of banks	8Banks	16Banks (4BG)
	Page size(X4/8/16)	1KB / 1KB / 2KB	512B / 1KB / 2KB
	# prefetch	8bits	8bits
	Added function	RESET/ZQ/Dynamic ODT	+ CRC/DBI/Multi preamble ..
Physical	Package type/balls (X4,8/X16)	78 / 96 BGA	78 / 96 BGA
	DIMM type	R,LR,U,SoDIMM	+ ECC SoDIMM
	DIMM pins	240 (R,LR,U) / 204 (So)	284 (R,LR,U) / 256 (So)

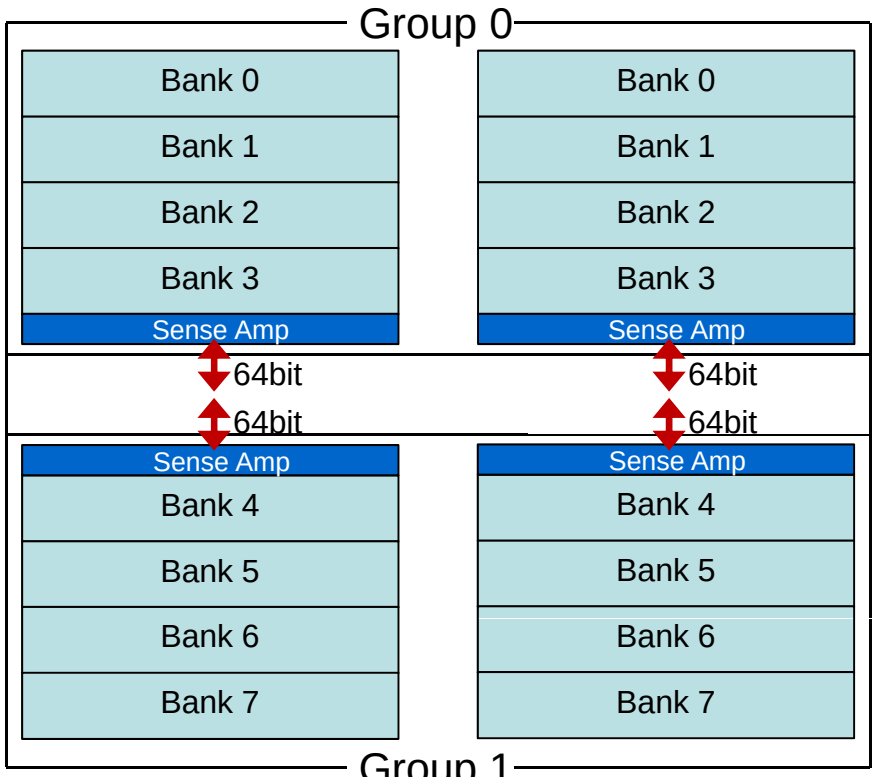
Bank Group

- **Bank Group alleviates the needs to increase core frequency from previous gen. products to DDR4**

	DDR	DDR2	DDR3	DDR4
BL	2	4	8	8 with BG
Core freq.	200MHz	200MHz	200MHz	200MHz



<X4/X8: 16 Banks with 4 Bank Group>

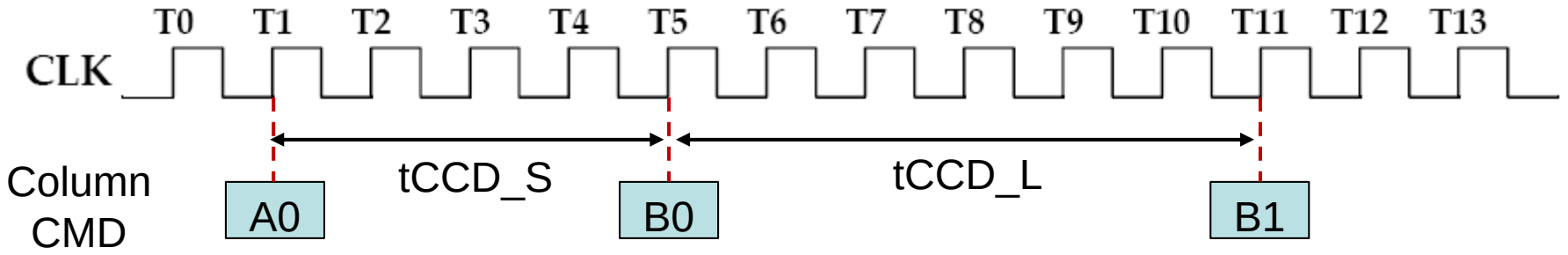


<X16: 8 Banks with 2 Bank Group>

Bank Group

- **Bank Group defines tCCD / tRRD parameters differently between same bank group and different bank group**

Data rate (Mbps)	1600	1866	2133	2400
tCCD_L (Diff BG)	5nCK	5nCK	6nCK	6nCK
tCCD_S (Same BG)	4nCK	4nCK	4nCK	4nCK



A0 & B0 are in different BG, B0 & B1 are in same BG

Fine Granularity Refresh

- As density increases, tRFC gets longer and limits performance
- Added new function supporting X2/X4 more frequent refresh with shorter tRFC

Ax	Ay	Az	Refresh rate mode
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	Reserved

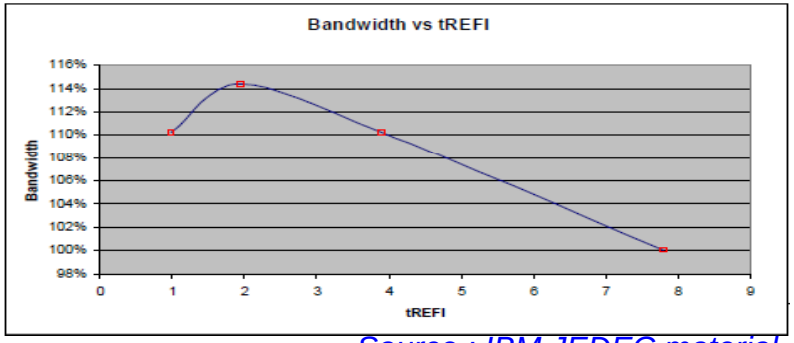
Table 23 — tREFI and tRFC parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Units
	tREFI(base)		7.8	7.8	7.8	TBD	usec
1X mode	tREFI1	0'C <= TCASE <= 85'C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	usec
		85'C < TCASE <= 95'C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	usec
	tRFC1		TBD	TBD	TBD	TBD	
2X mode	tREFI2	0'C <= TCASE <= 85'C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	usec
		85'C < TCASE <= 95'C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	usec
	tRFC2		TBD	TBD	TBD	TBD	
4X mode	tREFI4	0'C <= TCASE <= 85'C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	usec
		85'C < TCASE <= 95'C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	usec
	tRFC4		TBD	TBD	TBD	TBD	

- Fine granularity refresh shows better performance

tRFC	tREFI	BW
560ns	7.8us	1X
300ns	3.9us	1.03X
160ns	1.95us	1.05X
110ns	0.975us	1.02X
75ns	0.4875us	0.97X

Case: 2Gb based 2Rank system



Source : IBM JEDEC material

CRC(Cyclic Redundancy Check)

- **DDR4 supports WRITE CRC to assure better reliability in system**
  - **Data bits are followed by CRC bits**

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBI	d64	d65	d66	d67	d68	d69	d70	d71	1	1

<CRC data bit mapping for x8 device>

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	CRC4
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	CRC5
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	CRC6
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	CRC7

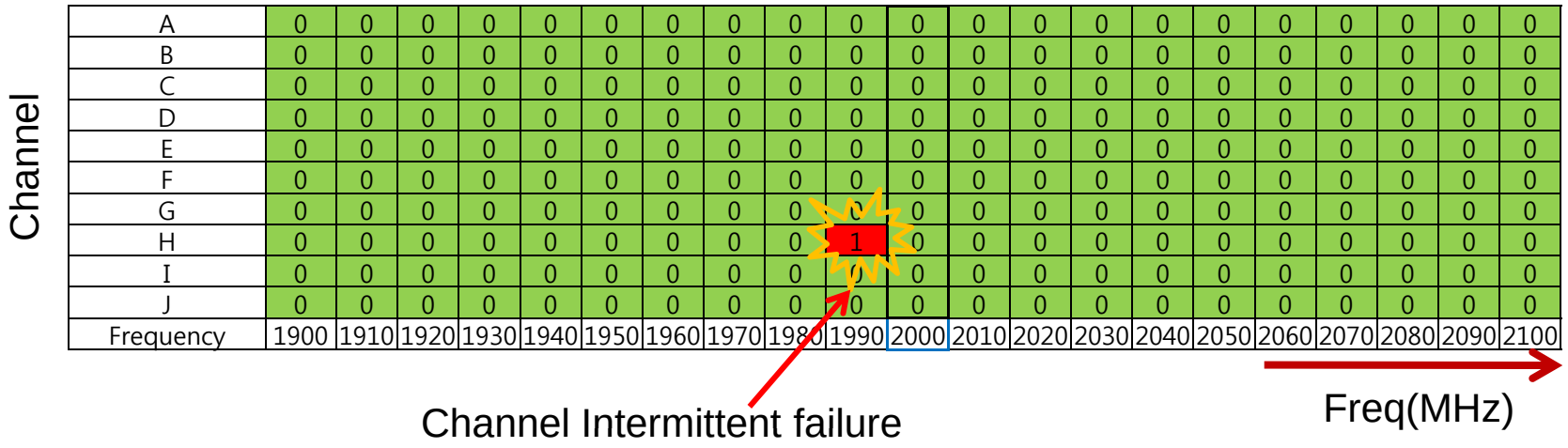
<CRC data bit mapping for x4 device>

- **CRC polynomial is the ATM-8 HEC (X^8+X^2+X^1+1) and 8 CRC bits are generated from 72 data+DBI bits**
  - **Same polynomial as GDDR5**
  - **In BC4 case, chopped 4UI will be treated as “1”**
  - **With CRC enabled, using burst ordering with A0:A1 is limited (Fixed to 0:0)**

Table 1. Error Detection Details	
ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC(Cyclic Redundancy Check)

- CRC fixes intermittent failure and realizes better system reliability
- About 10 % of performance gain is expected



DBI & DM

- **DBI : With DBI Enabled via MRS, DDR4 converts Data byte lane per UI. Therefore, it increases # of "1" which doesn't have DC current path in VDDQ Termination**

DQ[0:7] per UI	DBI	After Converting Data	# of "0" including DBI
0000_0000	0	1111_1111	1
0000_0001	0	1111_1110	2
0000_0011	0	1111_1100	3
0000_0111	0	1111_1000	4
0000_1111	1	0000_1111	4
0001_1111	1	0001_1111	3
0011_1111	1	0011_1111	2
0111_1111	1	0111_1111	1
1111_1111	1	1111_1111	0

- **DBI can be enabled separated for each READ/WRITE with MRS option**
- **If DM is enabled, then WRITE DBI is not supported**
- **For Read, CRC & DBI can be supported at the same time**

Table 1 DRAM Mode Register MRx

Ax	DM Enable
0	Enabled
1	Disabled

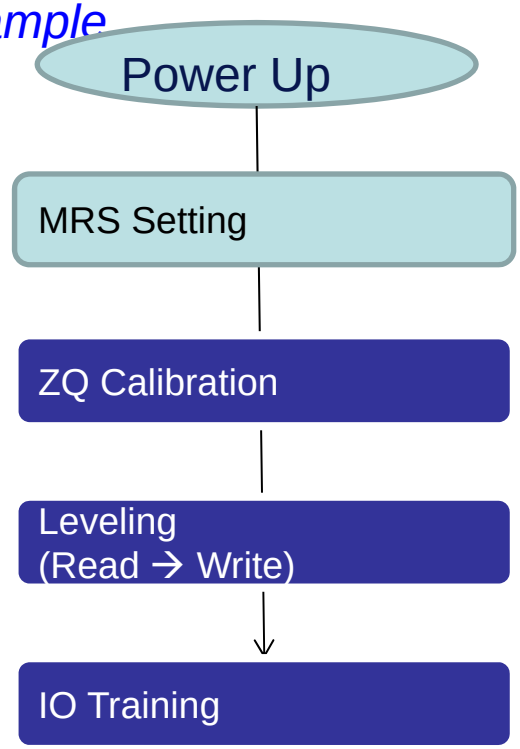
Table 2 DRAM Mode Register MRx

Ay	Write DBI Enable	Az	Read DBI Enable
0	Disabled	0	Enabled
1	Enabled	1	Disabled

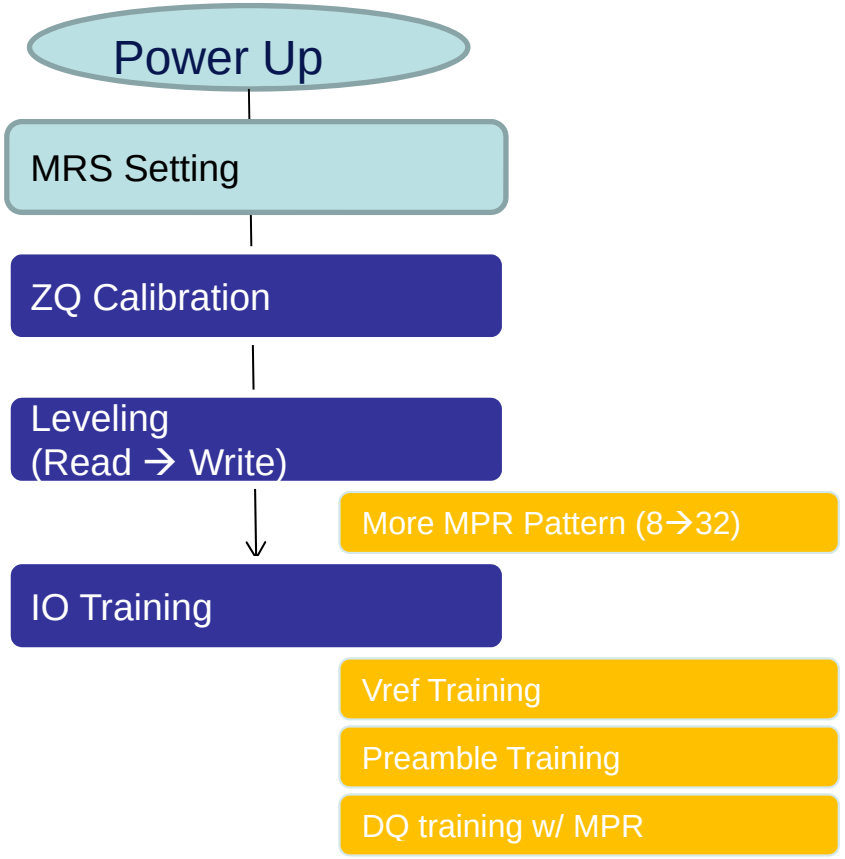
High Level Training/Calibration Flow

- **The following is example of training @initialization based upon supported function in JEDEC spec**
  - **Actual training/calibration sequence would be different depending on controller**

Current Typical DDR3 System Example

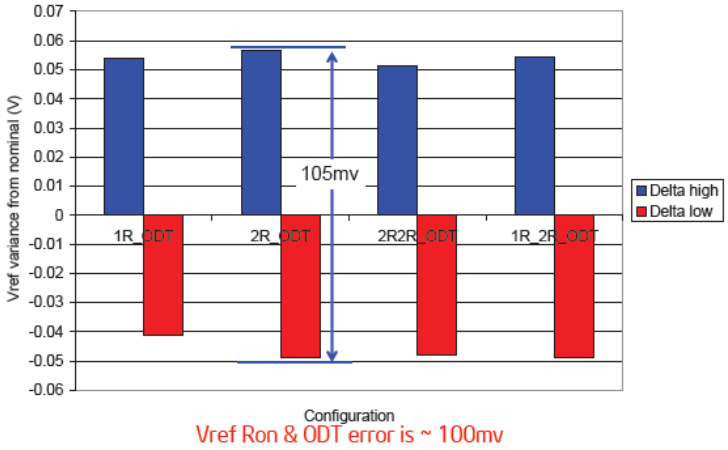


Expected DDR4 Flow



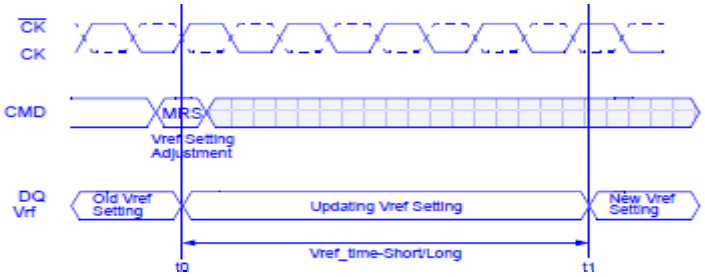
Calibration/Training : Vref & DQ

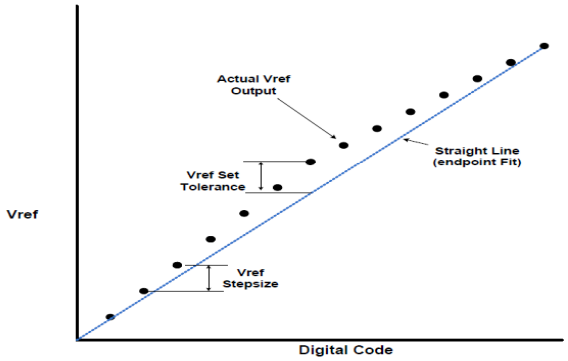
- **DDR4 changed data line termination from CTT to POD to save IO Power**
  - One downside of POD in multiple DIMM configuration, Vref level in each rank might be different



[source: DDR4 TG]

- **Therefore, DDR4 has internal VrefDQ which requires training from Host which requires at initialization**
  - Vref Step increase/decrease will be controlled via MRS Opcode
  - 1 Vref Step size is 0.65% of VDDQ
  - 1 Step or multiple step increase/decrease is allowed for efficient calibration time

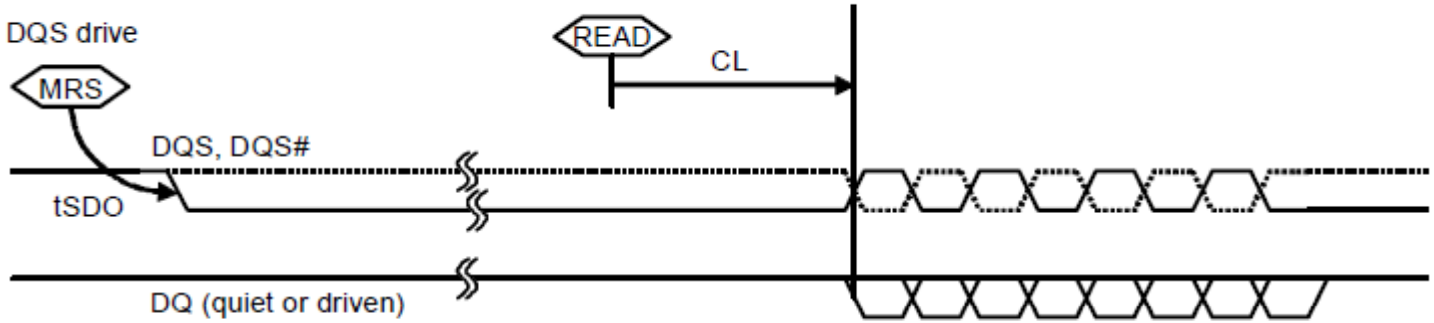




Calibration/Training : Preamble Training, MPR

- **DDR4 supports READ Preamble Training via MRS to have better fine alignment of HOST Rx enable time**
  - **With this mode, Host can detect when Host Rx should be enabled to get READ Data from DRAM**

Host enables Rx @ 1st edge : the edge will be different depending on board configuration



- **DDR4 assigned more MPR for DQ training and also it's Re-writable**
  - **DDR3 MPR is Read only**

	DDR3	DDR4	Note
# of MPR	8Bits (1Register)	**32bits (4Register)**	
Predefined Pattern	01010101	**MPR0: 01010101 MPR1: 00110011 MPR2: 00001111 MPR3: 00000000**	

Calibration/Training : Preamble Training, MPR

- **DDR4 Supports 3 way of DQ Link Training with 4 MPR as follows**

1) Serial Readout : Predefined pattern or Re-writed pattern is returned to Host Serial manner

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

2) Parallel Readout : Predefined pattern or Re-writed pattern is returned to Host Parallel manner

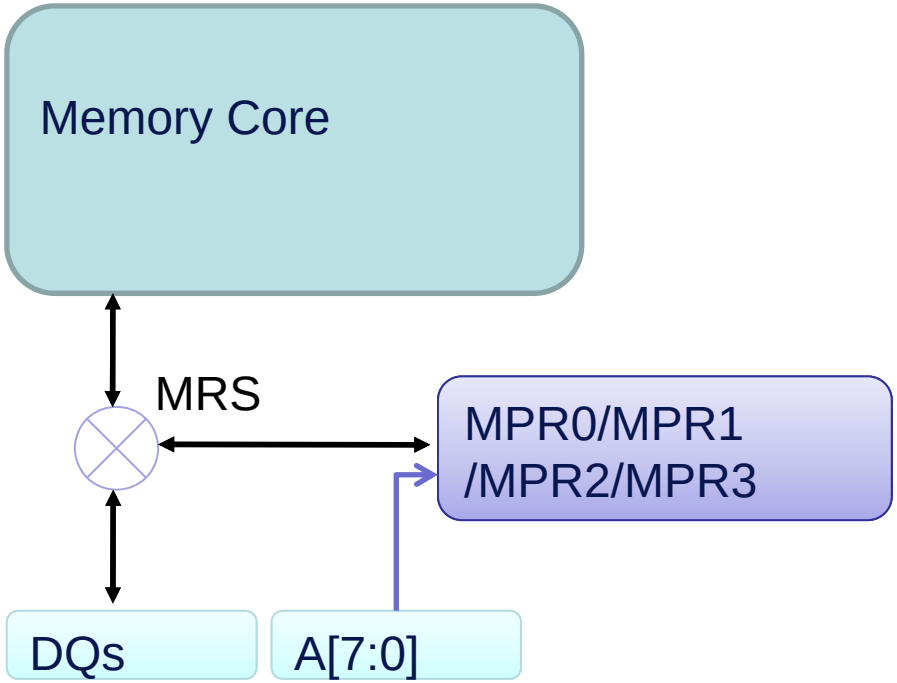
Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

3) Staggered Readout : Predefined pattern or Re-writed pattern is returned to Host Staggered manner as following

Stagger	UI0-7	UI8-15	UI16-23	UI24-31	UI32-39	UI40-47	UI48-55	UI56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2
DQ4	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ5	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ6	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ7	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

Calibration/Training : Preamble Training, MPR

- **MPR can be re-writed via Address Line**



Precharge All

MRS to set path to MPR

Write Command

-BA1/BA0 indicte the MPR Location
-- A[7:0] = Data for MPR

Read Command

- MR3 (A12,A11) to select Readout mode
- Serial / Parallel / Staggered