

Ultra Accelerator Link™ (UALink™) Consortium Publishes Four Specifications Defining In-Network Compute, Chiplets, Manageability and 200G Performance

UALink Consortium Achieves Key Milestones, Underscoring Industry Momentum for Open AI Scale-Up Interconnect Technology

Beaverton, Ore. – April 7, 2026 – The [UALink Consortium](#), the industry standards organization developing the open scale-up interconnect for next-generation AI workloads, today announces the ratification of the next UALink Specification, which encompasses three major additions – In-Network Compute, Chiplet Definition, and Manageability. The new specifications support the deployment of UALink solutions in multi-workload environments, while simultaneously helping improve UALink technology efficiency, performance for AI workloads and ease of implementation.

The UALink Consortium provides a standardized foundation for accelerator connectivity at scale, helping drive innovation, increase deployment flexibility and support the rapidly growing performance demands of next-generation AI workloads. The new specification update is facilitated through UALink Consortium’s open governance model, which fosters innovation while enabling a robust, multi-vendor supply chain, providing system designers and cloud providers with the necessary flexibility to deploy interoperable solutions without vendor lock-in.

“As AI workloads continue to outpace traditional interconnect timelines, we are pleased to deliver an essential update to the UALink Specifications,” said Kurtis Bowman, UALink Consortium Board Chair. “The advancements to UALink technology introduced in this release will enable the industry to quickly and efficiently integrate UALink solutions into their architectures. The UALink Consortium remains committed to advancing AI infrastructure through open industry standard technology that facilitates next-generation AI applications to the market.”

New UALink Specifications

- **UALink Common Specification 2.0**
 - Introduces In-Network Compute for UALink technology, facilitating computation and communication between accelerators.
 - Reduces latency, saves bandwidth, and improves scaling efficiency for distributed training and inference for AI solutions for complex and multi-workload environments for UALink systems.
- **UALink 200G Data Link and Physical Layers (DL/PL) Specification 2.0**
 - Split the DL/PL Specification from the UALink Common Specification to enable UALink to move quickly as new physical layers and speeds are needed by the industry without requiring changes to the other specifications.
- **UALink Manageability Specification 1.0**
 - Introduces UALink as a system with centralized control and management planes.
 - Utilizes standardized protocols, modeling and APIs like gNMI, Yang, SAI and Redfish.
- **UALink Chiplet Specification 1.0**
 - Defines the necessary information to integrate UALink technology into chiplet-based SoCs, including interfaces, form factors, flow control and chiplet management standardization.

- Fully compliant with the UCle® 3.0 Specification for simplified integration into existing chiplet ecosystems.

All of the UALink specifications are available for public download at <https://ualinkconsortium.org/specification/>

As UALink technology continues to advance, the Consortium plans to introduce interoperability and compliance programs designed to support a robust, multi-vendor ecosystem. Companies interested in advancing UALink technology and contributing to the development of these programs are encouraged to join the Consortium and help shape future UALink specifications. For membership information or to join, visit www.UALinkConsortium.org or contact admin@ualinkconsortium.org.

Additional Resources:

- [UALink Consortium Member Company Statements of Support](#)

About Ultra Accelerator Link Consortium

The Ultra Accelerator Link™ (UALink™) Consortium, incorporated in October 2024, is the open industry standard group dedicated to developing the UALink specifications, a high-speed, scale-up accelerator interconnect technology that advances next-generation AI & HPC cluster performance. The consortium is led by a board made up of stalwarts of the industry: Alibaba, AMD, Apple, Astera Labs, AWS, Cisco, Google, HPE, Intel, Meta, Microsoft, and Synopsys. The Consortium develops technical specifications that facilitate breakthrough performance for emerging AI usage models while supporting an open ecosystem for data center accelerators. For more information on the UALink Consortium, please visit www.UALinkConsortium.org

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